Single-Event Upset in the PowerPC750 Microprocessor

Gary M. Swift, Steven M. Guertin, Farhad F. Farmanesh, Farokh Irom, and Douglas G. Millward

I. Introduction

The effects of heavy ions and protons in space on advanced microprocessors are key problems in the design and planning of future spacecraft. Energetic heavy ions can disrupt the functional operation of microprocessors, and in some cases may cause catastrophic effects such as latchup to occur. Radiation tests of microprocessors are difficult and costly. Only a few microprocessors have been subjected to radiation tests and, because of the rapid pace of the commercial processor market, those results are for devices with larger feature sizes and higher operating voltages than current devices [1-6]. Of course, some results may exists which are considered proprietary.

A series of single-event tests were done to provide estimates of upset rates in various space environments, including earth orbiting, deep space and planetary exploration missions. The results also help determine what failure or upset modes dominate in highly-scaled, advanced processors.

In this paper we report results of single-event tests of the PowerPC750 from Motorola and IBM, which are manufactured with advanced processes that uses a minimum feature size of 0.29 and 0.26 μm, respectively. This report includes test results for all program-visible PowerPC750 registers, the L1 caches and their tags, the L2 tags, and the page table buffer as well as overall results for processor functionality. A series of tests was done using two different types of radiation sources: energetic protons, which have sufficient range to penetrate the packaging material of the PowerPC750, and heavy ions, which have limited range, and require tests on specially prepared samples that have been thinned so that the ions can penetrate to the front side of the die using irradiation from the back.

The test approach was based on commercially available development boards that provide much of the hardware required to make the processor operational. A monitor/debugger, essentially a simplified operating system, was provided with the test boards and was used to load and start execution of the test programs. These were used to select and load patterns into the various sections of the processor before irradiation and monitor or report the upset results.

II. Background on the PowerPC750

PowerPC750s are available from several manufacturers that are architecturally identical. Originally, this family of processors was designed by a consortium of Apple, Motorola, and IBM. Although Motorola and IBM use different foundries for making them, they are kept identical as far as possible, even to the feature arrangement on the die floorplan; IBM's is shown in Figure 1. The dimensions of the IBM PPC750 are 7.6 mm x 8.8 mm while the Motorola XPC750's are 8.5 mm x 9.4 mm. While the Motorola die is ~20% larger in overall area due to its 10% larger linear feature size, the fraction of the area occupied by each corresponding functional unit is the same.

The main elements and their relative areas can be seen in Figure 1. The left half of the chip is mostly execution units while the right half has the larger memory arrays delineated. Table I lists the memory elements tested for single event upsets; except for the registers, their relative areas are shown in the Figure which is taken from a summary sheet available on the webpage: www.chips.ibm.com .

The tested PowerPC750s have more than 6.3 million transistors, run at up to 300MHz, and dissipate less than 6.5Watts using a 2.5V core with 3.3V interface pins. Unfortunately for heavy ion testing, it is packaged in a 360-pin BGA (ball grid array) package in a "flip-chip" configuration where bump bonding interconnects the die to the package. Thus, it is necessary to irradiate through the silicon substrate to reach the active layer, and it is desirable to thin the silicon so that ordinary ground-test beams may be used.

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III. Experimental Method

We used Motorola's PowerPC evaluation board known as "Yellowknife" as a test platform. This board was chosen because it eliminates the large engineering effort required to design a custom test board for the processor and also provides a very basic internal operating system that eliminates the many layers of code in more advanced operating systems. This provides far better timing, diagnostic information and control of processor information flow. The Yellowknife has a ZIF (zero insertion force) socket which accommodates a small daughter card for the processor and cache chips. There are no active components nearby or underneath which is important for penetrating proton irradiation (this allowed us to shield other components on the board during proton tests, assuring that the measured response was entirely due to effects within the processor). The Yellowknife board comes with a simple monitor/debugger that Motorola has dubbed DINK. Although the board has many features associated with a Personal Computer motherboard, including PCI and ISA slots, floppy and IDE disk controllers, a keyboard connection and multiple I/O ports, these are mostly not supported by DINK and so were not used. DINK communicates over a bi-directional serial port to a computer terminal. The other external communication provided on the Yellowknife that we used is a JTAG port (JTAG is an industry standard, boundary scan interface). An Agilent Technology 5900B JTAG probe was used to interrogate the processor and memory even after unexpected events occurred such as operational errors during irradiation.

Two main test methodologies were developed: (1) the "do little" method and (2) the "pin wiggler" method; these designations refer to the processor activity during irradiation. In the classification system of Koga et al. [8], both techniques are variants of Method 1, a self-testing single computer, although the JTAG probe adds elements of "controller assisted" Method 2. As noted in Reference 8,running the processor at full speed is the main advantage compared to other approaches, although it was subsequently shown that the "golden chip" approach could be run at speed [9]. Slowing down the clock would not change the static register susceptibilities, but is necessary to determine if the upset rate is dominated by clock tree hits and transients in combinational logic.

In the "do little" method, the processor performs a single-instruction infinite loop interrupted briefly every half second to write a register snapshot to a strip chart in the physical memory. The repeated execution of a one word instruction that always branches back to itself minimizes processor activity and reduces the number of internal operations, thereby making the operation susceptible to errors in only a few internal locations. Even program counter upsets are trapped (via a "system call" instruction) and counted and the loop is re-entered. After the irradiation has ended, an external interrupt triggers a reporting subroutine and enables downloading the strip chart.

In the "pin wiggler" method, the processor is programmed to perform a self-inspection of one of its internal register files or memory arrays, and to toggle an address pin if an error is found. The "pin wiggler" method has the advantage of providing active, continuous feedback to the experimenter during the irradiation while the "do little" method is essentially blind until the test run has been completed. A set of external hardware counters was used to monitor the wiggling pins on the Yellowknife board to determine if any changes occurred during the irradiation. The lines were coded to indicate (a) whether the main software loop was still functioning properly; (b) if an upset had just been detected; and (c) whether the half-second interrupt continued to function.

More complex methods were required to examine errors in the L1 data and instruction caches. The two types of caches were initialized in specified conditions prior to irradiation. Both caches were then disabled. Then a clearly recognizable pattern *designed to be distinctly different from the content of the cache* was placed in the external memory space covered by the caches. Verification of the cache contents was done by comparing the cache contents after irradiation with the pattern initially loaded. Examination of the instruction cache was only possible using the JTAG interface, examining the instruction cache to determine its contents. Tag upsets (as well as upset of the data valid flag) were detected by monitoring for the distinctly different pattern. The tag and data valid upsets were thus distinguished and counted separately from upsets of the data bits themselves.

Additional test programs were developed that used the floating point unit within the processor. Those tests were done in order to determine whether transient logic errors within the floating point unit would cause the error rate to increase. This provided an indirect method to evaluate transient logic errors because the floating point unit contains a very large array of combinational logic.

Proton tests are far more straightforward than tests with heavy ions because the tests can be done in air, without any need for package modification or vacuum chambers. Proton tests with energies above 65 MeV were performed at the Indiana University Cyclotron Facility. Tests at lower energies were done at the UC Davis cyclotron.

Heavy-ion testing is more complicated than proton testing because the "flip-chip" design of the PowerPC750 does not allow the device to be "delidded" in the usual sense without destroying the pad and bonding connections. The limited range of ions from most ground-test facilities does not allow them to penetrate the package. Although it is possible to use ions with extremely energetic beams to overcome this problem, such facilities are extremely costly and difficult to schedule. We were able to test with ions accelerated by the Texas A & M Cyclotron by milling away part of the back surface of the PPC750, reducing the thickness of the die from 712 μm to 50-200 μm. Several thicknesses were used to address the concern that, if the die was too thin, it might

affect the charge collection. With the thinner dice, heavy ions from a low energy accelerator are able to penetrate the active region. The upset mechanism requires penetration of the ion beyond the top surface of the die. The Texas A&M accelerator was used because they provide longer range ions than other available heavy ion facilities. Much of this testing was done by placing the entire Yellowknife board and JTAG probe in the vacuum system; however, the longer range ions do permit the use of in-air irradiations, so this was done in recent tests. The processor and other components on the board must dissipate considerable amounts of power, and tend to overheat especially in vacuum. The data presented here was collected by allowing time for the processor to cool between successive irradiation when needed. A custom heatsink with a hole for the processor die was used to conduct heat away from the package and a thermocouple was used to measure temperature increases during the time that the device operated within the vacuum system. Later, a routine to read out the processor's junction temperature was developed.

IV. Proton Test Results

The first tests that were done with protons were successful in identifying errors in registers, but the test results were occasionally disrupted by program "hangs". This was partly due to the implementation method used in the initial tests, which effectively relied on successful processor operation to identify internal errors. Program "hangs" were also observed in earlier tests of other microprocessor types [1-6], and are difficult to deal with.

One way to deal with the "hang" problem was to use the "pin wiggler" method to continually monitor status and errors during each run. Figure 2 shows an example.

In this figure, errors develop in a nearly linear way as the test progresses. This shows that there are no significant error bursts, and that the error event rate is nominally proportional to the incremental proton fluence. However, near the end of the test run the processor "hangs", which is evident by the loop counter response as well as sudden saturation of the errors. Although this approach does not eliminate "hangs" it allows valid data for part of a test run to be extracted from the run, as well as providing information about error propagation from the processor.

With this approach, we were able to measure the error rate for different types of internal registers at various proton energies. Figure 3a shows the results for the floating-point registers, with logic "1" stored; thus, the errors represent transitions from "1" to "0". The threshold energy is below 20 MeV, the lowest energy tested and the saturated cross sections are the same at both proton facilities.

The cross section for "1" to "0" errors saturated at about 10^{-13} errors-cm^2/p-bit. For the opposite transition ("0" to "1"), the error rate was consistently lower by about a factor of 3, excepting one data point (see Figure 3b). This asymmetry is not unusual for minimum-area, statically-implemented registers.

Test results for the general-purpose and special-registers were very similar to the results obtained for the floating-point registers, with nearly the same saturation cross section. However, the threshold energy for the general-purpose registers and special-purpose registers were slightly higher with some difference in the curve shape.

Results for the data cache bits were significantly different, as shown in Figure 4a. First, the decrease in cross section occurs at energies that are considerably lower than that of the other registers cache. The saturation cross section is nearly a factor of two lower. The threshold behavior is likely the result of implementing dynamic storage to reduce the bit area (there are 256K bits in each L1 cache). Thus, the critical charge required for upset is reduced. The lower saturation cross section is probably due to reduced bit area. The IBM PPC750 has an almost identical proton upset response, as can be seen in Figure 4b.

The data cache tags and the "data valid" flags had similar responses during proton tests, as shown in Figure 5. The instruction cache results indicate that it also had a similar response to protons.

It is also interesting to compare our results for the 0.29 μm Motorola PowerPC750 with older results for the PowerPC603 [5] which has a feature size of 0.4 μm and represents the previous generation of advanced microprocessors from Motorola; see Figure 6. The data cache error rate for the PPC750 is about a factor of three lower than that of the PPC603, with (perhaps) comparable energy thresholds for the two types of processors. Thus, the increased speed and higher density of the PPC750 does not appear to have increased the sensitivity of the registers to upset from protons.

V. Heavy Ion Test Results

As discussed in the Introduction, heavy ion tests are far more difficult to do with advanced processors because of the difficulty of getting ions to penetrate the flip-chip package assembly. Heating of processors during the test within the vacuum system is also a problem. The PPC750 dissipates about 5W during normal operation running the test programs. Even the specification maximum of 6.5W is considerably lower than the power dissipation of competing high-speed processors, such as the Pentium III which runs closer to 50W. We were able to use a heat sink on the package to provide cooling to the device during tests and monitored the package temperature with a thermo-couple and the junction temperature with a special subroutine taking advantage of a provided PPC750 capability.

Figure 7 shows the dependence of the heavy ion cross section on LET for the special-purpose registers (results for other types of registers exhibited similar but not identical behavior). The cross section increased rapidly from about 10^{-9} cm^2/bit to approximately 10^{-7} cm^2/bit at higher LET values.

The data in Figure 7a show an independence of data pattern for the Motorola part, similar to that shown by the proton results for the data cache. The IBM device is also independent of pattern, as shown in Figure 7b. In contrast the data of Figure 8a, the cross section for the floating point registers, shows an asymmetry with upsets of "1s" about twice as likely as "0s," in general agreement with the factor of three seen earlier in the proton results.

There are many different data points in the curves of Figure 7 and 8, with a number of different test conditions and two different test methods. Several different parts were used, with thicknesses of 50, 100 and 200 μm. The LET at the device surface is corrected for the decrease in beam energy as the ions traversed the device. Unlike the convention for front-side irradiation the assigned LET is the exit LET, not the incident LET. Note that the incident beam energies were chosen so that the exit energy is well above the Bragg peak value.

There is good agreement in the results for the different devices after the transport correction. This appears to validate the backside irradiation technique for these processors, although in this case we do not have irradiation data from the top for comparison. One would not expect major charge collection differences between these thinned devices because advanced processors require a fairly thin epitaxial layer.

It is interesting to compare the heavy ion results with the PPC603 results of Bezerra, et al. [5] as shown in Figure 9. The threshold LET is about the same as for the PPC603e, but again the "saturation" cross section is significantly lower for the XPC750. Thus, the increased scaling and decreased internal operating voltage of the XPC750 have somewhat lowered the SEU sensitivity.

Processor hangs "interfered" with both the proton and heavy ion testing for both the Motorola and IBM devices at about the same rate. Some types of hangs responded to a hard reset and some did not. Defining a hang as a failure to respond to an external interrupt, the device cross section observed across these tests is about 10^{-5} cm^2 for LETs above about 5 MeV per mg/cm^2.

VI. Conclusions

The experimental results presented here can be used directly to calculate the upset rates of the *test* programs if they were run in a space radiation environment. However, *real* applications are more complex, and accurate space-rate predictions would require detailed information on the use and duty cycles of the various internal registers, caches and execution units. Although this could be done in principle, a simpler approach is to bound the rates by assuming 100% duty cycle of the elements used. This bound should be valid if the processor is dominated by direct memory element upsets, not single-event transients. Except for the hangs, this is clearly the case for the PowerPCs tested here. The application-like results presented in Reference 5 are considerably lower than their register and cache results, showing it is true for the earlier PowerPC 603e as well.

These results show that single-event upset susceptibility in advanced commercial processors is actually somewhat improved compared to an earlier generation of the same processor family, allowing them to be used in space applications where occasional malfunctions can be tolerated. Although comparisons of register upset rates are a useful way to examine single-event susceptibility, the more difficult issue is how frequently more complex malfunctions of the processor occur, and how they can be detected and corrected when more complex operating systems are used. Interestingly, these "hangs" were much less frequent than seen for Pentium processors [6], particularly after trapping beam-induced exceptions, program counter hits, and mis-branching; it is not clear that these useful test techniques would be able to be implemented in flight software. Nevertheless, the low space rates, combined with reasonable total dose and immunity to latchup and relatively low power consumption, make the PowerPC750 a useful candidate for non-critical, highly-computational tasks in space.

VII. References

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	# of bits
Registers:	
General Purpose Registers (GPRs)	1024
Floating Point Registers (FPRs)	2048
Special Purpose Registers (SPRs)	2560
L1 Cache:	
Data (D-cache)	256K
Data Tags and Flag	30K
Instruction (I-cache)	256K
Instruction Tags and Flag	30K
L2 Tags and Flag	120K
Page Table Cache (TLBs)	8K

Table I. Tested Memory Elements of the PowerPC750

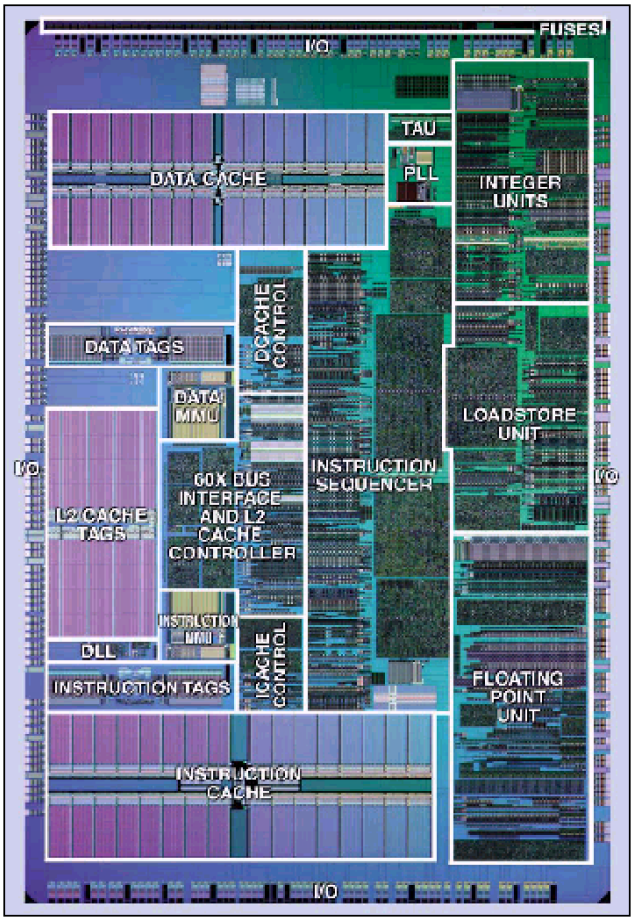

Figure 1. Die photo of the IBM PowerPC750 with overlay showing major functional and storage units (from the IBM website).

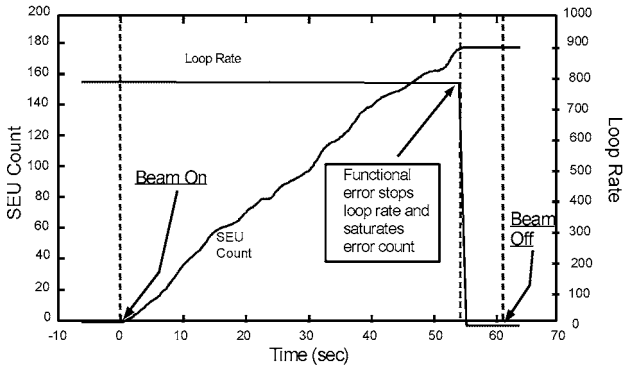

Figure 2. Error count accumulation and processor status information during a test run using the "pin wiggler" method.

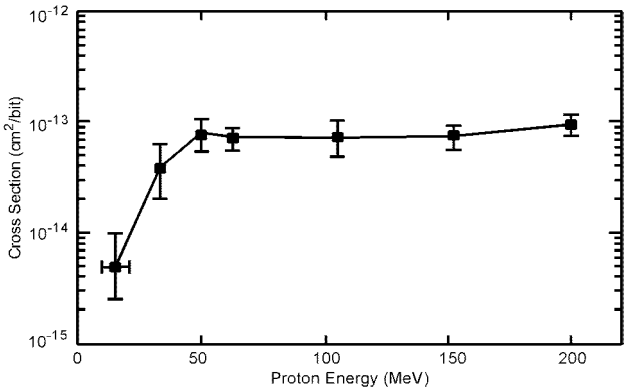

Figure 3a. Cross section vs. proton energy for "1" upset to "0" in the floating point registers in the Motorola Power-PC750. Note that the three data points at energies higher than 100 MeV were measured at Indiana, the rest at UC-Davis. Vertical error bars are ~2 sigma and result from Poisson counting statistics.

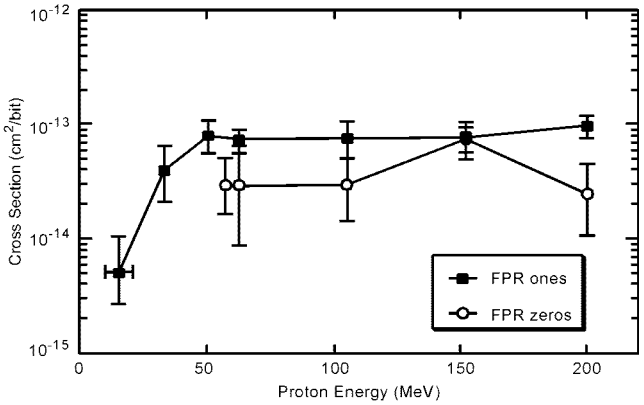

Figure 3b. Cross section vs. proton energy for a "0" upsetting to "1" in the floating point registers in the Motorola PowerPC750 compared with the cross sections for the opposite direction upset.

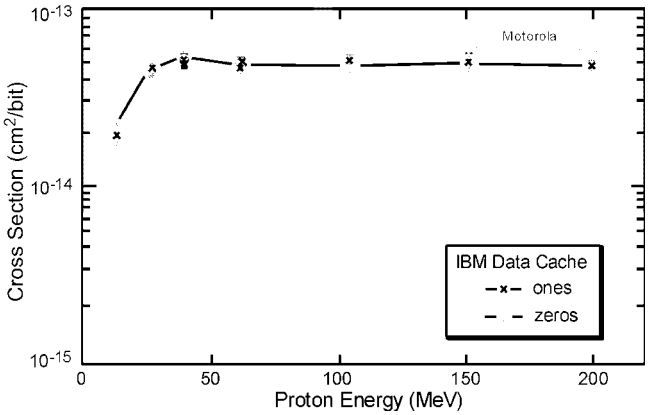

Figure 4b. Comparison of the proton upset susceptibility of the IBM PPC750 data cache to the Motorola XPC750.

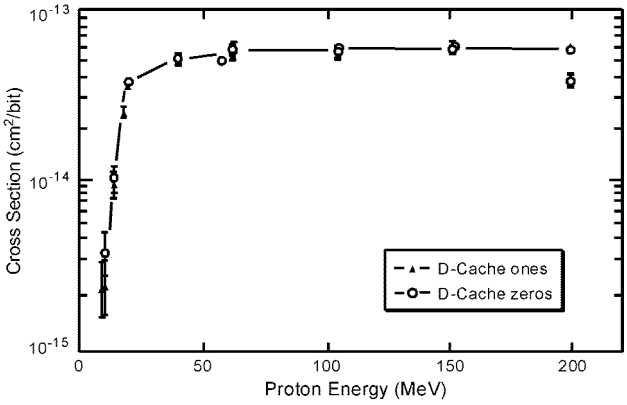

Figure 4a. Pattern independence of the data cache bits: Measurements of the proton upset susceptibility for the Motorola XPC750 data cache bits storing "one" are statistically indistinguishable from when storing "zero." Note some error bars are smaller than the plotting symbols.

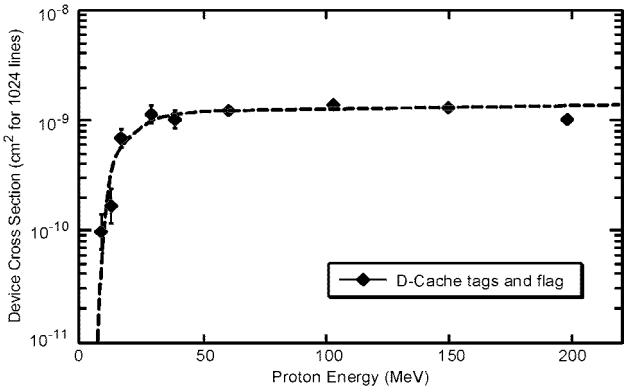

Figure 5. The proton upset cross section for the Motorola XPC750 data cache tags and data valid flags. The dashed curve is only a guide for the eye.

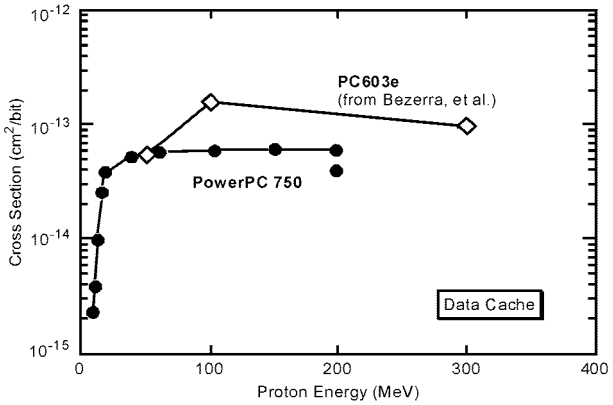

Figure 6. Comparison of the present results on the Motorola PowerPC750 with earlier results on the Motorola PowerPC603e from Reference 5.

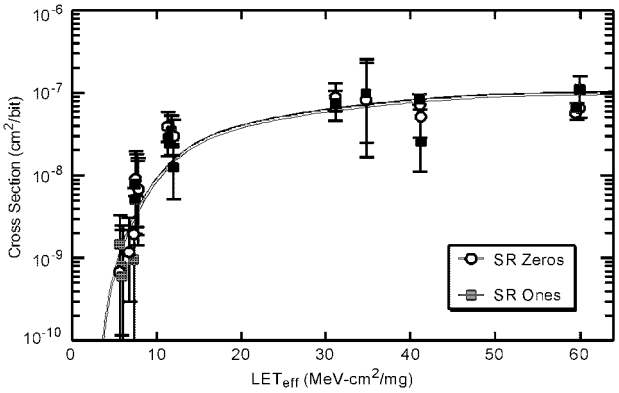

Figure 7a. Heavy-ion upset cross section for special-purpose registers in the Motorola PowerPC750. There is so little pattern dependence that the curves (fitting the one-parameter, physics-based equation of Ref. 9) are on top of each other.

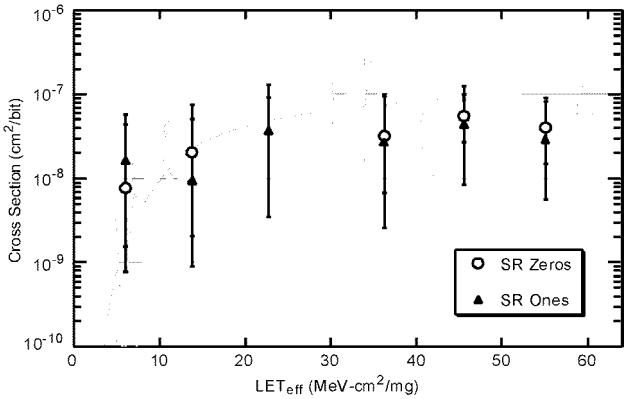

Figure 7b. Comparison of the heavy ion upset cross section of the IBM PPC750 special purpose registers to the Motorola XPC750.

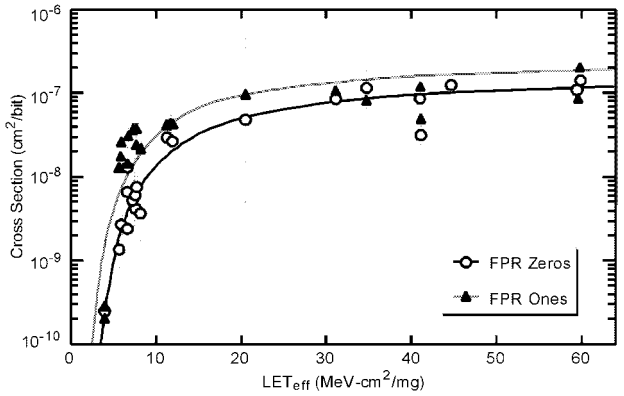

Figure 8a. The heavy-ion cross section for the floating point registers of the Motorola PowerPC750 comparing the susceptibility of upsetting ones with that for zeros.

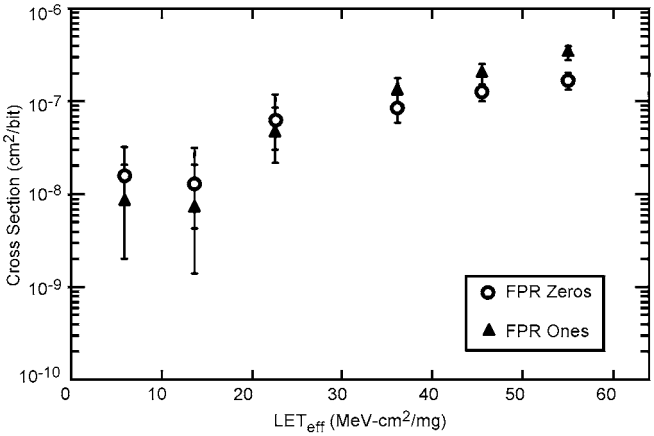

Figure 8b. Comparison of the heavy-ion cross section for the IBM PowerPC floating point registers with those of the Motorola PowerPC750.

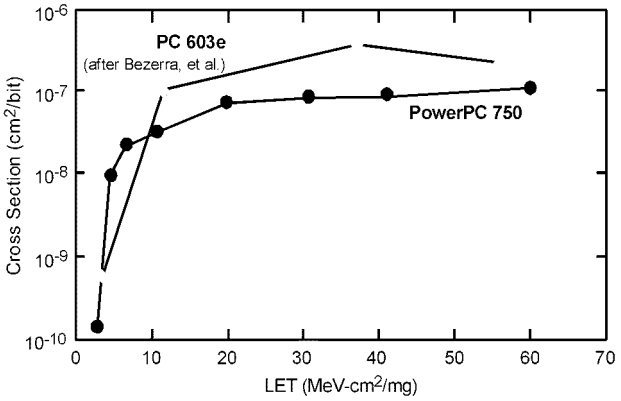

Figure 9. A comparison of the present results for the Motorola PowerPC750 with earlier register results for the Motorola PowerPC603e.